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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,219	02/24/2004	Toshihiko Uno	60188-775	8351

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,219	UNO, TOSHIHIKO	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/307,361.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/307,361, filed on December 2, 2002.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Wolf, *Silicon Processing for the VLSI Era*. Applicant teaches in prior art figure 11 and discussion on pages 3-5 of the specification that the prior art method includes a first step of implanting a semiconductor substrate 16 of a first conductivity type with an impurity ion of a second conductivity type, the implantation at an energy so as to form an extended drain region 23 of the second conductivity type in an upper portion of the substrate; and

a second step of forming a plurality of buried layers 18A and 18B, each being an impurity layer of the first conductivity type, in the extended drain region so that the plurality of buried layers extend substantially parallel to a substrate surface with an interval therebetween in a depth direction.

The admitted prior art teaches that the first implantation step is performed at an energy of between 100 to 150 keV (page 5, lines 1-2) rather than the claimed energy of about 1.0 to about 3.0 MeV. However, the admitted prior art also teaches that the lower implantation energy (100 – 150 keV) caused high resistance at the deeper regions (25, 26) of the extended drain region 23, (page 5, lines 2-5) which caused the overall resistance of the extended drain region to be greater than desired (page 4, lines 21-23). In light of this known defect, it is considered obvious to increase the implantation energy of the dopant ion since doing so will cause a deeper implant into the extended drain region and thus a higher concentration of impurity ions at the deeper regions 25 and 26. It is well known in the art that higher implant energy causes the depth or range R_P of the dopant ion to increase; Wolf teaches this in figure 7 on page 290. Specifically, Wolf teaches the range versus implantation energy for three species of dopant ions including phosphorous (P) which is used in the prior art to form the extended drain region (page 4, line 26). It is seen that at higher implantation energy (e.g. 1000 keV or 1.0 MeV), phosphorous achieves a deeper projected range; Wolf further teaches equation 7 on page 289 which determines ion concentration n at a depth x, and shows that ion concentration reaches a maximum at $x = R_P$. As such, the higher implantation energy achieves higher concentration at a deeper region. In turn, the higher impurity concentration achieves lower resistance (see Wolf, p. 28, Fig. 22). As such, it is considered obvious to use higher implantation energy with the dopant ion of the prior art to

achieve lower resistance in a deeper region of the extended drain; it was well known at the time of the invention that higher energy caused greater implantation depth, which further causes lower resistance at the greater depth.

The admitted prior art also teaches that the junction depth is between 5 – 15 μm and teaches or makes obvious the formation of the lower buried layer prior to the more shallow buried layer.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,168,983 to Rumennik et al. in view of 6,072,216 to Williams et al. Rumennik teaches in figures 11a-e and text beginning at column 9, line 44 a method of forming a device comprising:

a first step of selectively implanting a substrate 121 of a first conductivity type (P-) with impurity ion of a second conductivity type (N) to form an extended drain region 123 of the second conductivity type in an upper portion of the substrate; and

a second step of forming a plurality of buried layers 150 (fig. 11e), each being an impurity layer of the first conductivity type (P), in the extended drain region so that the buried layers extend parallel to a substrate surface with an interval therebetween in a depth direction. Rumennik also teaches that the extended drain is formed to a depth of 5 – 15 μm (col 9, lines 56-58) and that the lowermost buried layers are formed first (col. 11, lines 13-18).

Rumennik teaches that the first implantation is performed at an energy of 100 – 150 keV rather than at the higher claimed energy of about 1.0 to about 3.0 MeV. Williams teaches in figures 8G-I implanting a buried layer 404 to form part of an extended drain 112 and that the buried layer 404 is implanted at an energy of 0.5 – 3.0 MeV (col. 8, lines 1-7). Rumennik and

Williams are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Rumennik with an energy as taught by Williams. The motivation for doing so, as is taught by Williams, is that formation of such a buried layer reduces the on-resistance of the device (col. 4, lines 1-5). Therefore, it would have been obvious to combine Rumennik and Williams to obtain the invention of claims 5-7.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Imam et al. is cited for teaching a DMOS device having p-regions 202 formed in n-type extended drain 113 and that the extended drain may have increased doping to achieve a lower on-resistance (col. 3,lines 23-25).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax number is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER